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In Re Application of:

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For: Apparatus And Method For Power Efficient Line Driver

ALLOWED CLAIMS
Notice of Allowance mailed June 22, 2005

1. -39. (Cancelled)

40. (previously presented) A method comprising:

a) driving a first current through a line and a termination resistance so that a logical value on said line changes from a first logical value to a second logical value, said first current sustained for a width of a first bit that is propagated on said line; and,

b) holding said second logical value on said line by driving a second current through said line and said termination resistance, said second current less than said first current, said second current sustained for a width of a second bit that is propagated on said line.

41. (previously presented) The method of claim 40 wherein said first and second currents flow in a direction from said line into said termination resistance.

42. (previously presented) The method of claim 41 wherein said second logical value is a logical high.

43. (previously presented) The method of claim 41 wherein said first current produces a first voltage on said line that is larger than a second voltage produced on said line by said second current.

44. (previously presented) The method of claim 40 wherein said first and second currents flow in a direction from said termination resistance into said line.

45. (previously presented) The method of claim 44 wherein said second logical value is a logical low.

46. (previously presented) The method of claim 44 wherein said first current produces a first voltage on said line that is smaller than a second voltage produced on said line by said second current.

47. (previously presented) The method of claim 40 wherein said first bit width is coextensive with a clock cycle.

48. (previously presented) The method of claim 40 wherein said driving a first current further comprises applying a first multiplexer select line state to a multiplexer so that a first word is provided at an output of said multiplexer, said first word enabling a first number of sub-drivers, and said driving a second current further comprises applying a second multiplexer select line state to said multiplexer so that a second word is provided at said output of said multiplexer, said second word enabling a second number of said sub-drivers, said first number greater than said second number.

49. through 70. (canceled).

71. (previously presented) An apparatus to drive a logic level with multiple current strengths, comprising:

a plurality of drivers each having a enable/disable input, each said enable/disable input coupled to an output of a multiplxer, said mutliplexer having a first group of inputs and a second group of inputs, said first group of multiplexer inputs to provide an indication of a first number of said drivers to be enabled while driving a logic level with a first current strength, said second group of multiplexer inputs to provide an indication of a second number of said drivers to be enabled while driving a logic level with a second current strength.

72. (previously presented) The apparatus of claim 71 wherein said first number is greater than said second number and said first current strength is greater than said second current strength.

73. (previously presented) The apparatus of claim 71 wherein said first group of multiplexer inputs are coupled to a group of register outputs.

74. (previously presented) The apparatus of claim 71 wherein said multiplexer's channel select input is coupled to a signal line, said signal line to carry a signal that indicates when said logic level is to be driven with said first current strength and when said logic level is to be driven with said second current strength.

75. (previously presented) The apparatus of claim 72 wherein each driver of said plurality of drivers also has a second enable/disable input, each of said enable/disable inputs to enable/disable a P channel transistor within its respective driver, said P channel transistor to push current over a line, each of said second enable/disable inputs to enable/disable an N channel transistor within its respective driver, said N channel transistor to pull current from said line, said second enable/disable inputs coupled to an output of a second multiplexer.

76. (previously presented) The apparatus of claim 75 wherein said second mutliplexer has a first group of inputs and a second group of inputs, said first group of multiplexer inputs to provide an indication of a first number of said drivers to have

an enabled P channel transistor while driving said logic level with a first current strength, said second group of multiplexer inputs to provide an indication of a second number of said drivers to have an enabled P channel transistor while driving a logic level with a second current strength, said first group of second multiplexer inputs to provide an indication of a first number of said drivers to have an enabled N channel transistor while driving said logic level with a first current strength, said second group of second multiplexer inputs to provide an indication of a second number of said drivers to have an enabled N channel transistor while driving a logic level with a second current strength.

77. (previously presented) The apparatus of claim 76 wherein said first group of first multiplexer inputs are coupled to a first group of first register outputs and said first group of second multiplexer inputs are coupled to a second group of register outputs.

78. (previously presented) The apparatus of claim 76 wherein a first channel select input of said first multiplexer and a second channel select input of said second multiplexer are both coupled to a signal line, said signal line to carry a signal that indicates when said logic level is to be driven with said first current strength and when said logic level is to be driven with said second current strength.

79. (previously presented) An apparatus, comprising:

a DDR memory comprising address lines that are coupled to a plurality of drivers, each of said drivers having an enable/disable input, each said enable/disable input coupled to an output of a multiplexer, said mutliplexer having a first group of inputs and a second group of inputs, said first group of multiplexer inputs to provide an indication of a first number of said drivers to be enabled while driving a logic level with a first current strength, said second group of multiplexer inputs to provide an indication of a second number of said drivers to be enabled while driving a logic level with a second current strength.

80. (previously presented) The apparatus of claim 79 wherein said first number is greater than said second number and said first current strength is greater than said second current strength.

81. (previously presented) The apparatus of claim 79 wherein said first group of multiplexer inputs are coupled to a group of register outputs.

82. (previously presented) The apparatus of claim 79 wherein said multiplexer's channel select input is coupled to a signal line, said signal line to carry a signal that indicates when said logic level is to be driven with said first current strength and when said logic level is to be driven with said second current strength.

83. (previously presented) The apparatus of claim 80 wherein each driver of said plurality of drivers also has a second enable/disable input, each of said

enable/disable inputs to enable/disable a P channel transistor within its respective driver, said P channel transistor to push current over a line, each of said second enable/disable inputs to enable/disable an N channel transistor within its respective driver, said N channel transistor to pull current from said line, said second enable/disable inputs coupled to an output of a second multiplexer.

84. (previously presented) The apparatus of claim 83 wherein said second mutliplexer has a first group of inputs and a second group of inputs, said first group of multiplexer inputs to provide an indication of a first number of said drivers to have an enabled P channel transistor while driving said logic level with a first current strength, said second group of multiplexer inputs to provide an indication of a second number of said drivers to have an enabled P channel transistor while driving a logic level with a second current strength, said first group of second multiplexer inputs to provide an indication of a first number of said drivers to have an enabled N channel transistor while driving said logic level with a first current strength, said second group of second multiplexer inputs to provide an indication of a second number of said drivers to have an enabled N channel transistor while driving a logic level with a second current strength.

85. (previously presented) The apparatus of claim 84 wherein said first group of first multiplexer inputs are coupled to a first group of first register outputs and said first group of second multiplexer inputs are coupled to a second group of register outputs.

86. (previously presented) The apparatus of claim 84 wherein a first channel select input of said first multiplexer and a second channel select input of said second multiplexer are both coupled to a signal line, said signal line to carry a signal that indicates when said logic level is to be driven with said first current strength and when said logic level is to be driven with said second current strength.